Transceiver SI Development Kit, Stratix II GX Edition

Getting Started User Guide

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Contents

Appendix A. Non-GUI Based Example Design

About this User Guide

Revision History

The table below displays the revision history for the chapters in this user guide.

Chapter	Date	Version	Changes Made
All	June 2006	1.0.0	First publication

This user guide provides getting started information about the Altera® Stratix® II GX EP2SGX90 signal integrity development board.

How to Contact Altera

For the most up-to-date information about Altera products, go to the Altera world-wide web site at www.altera.com. For technical support on this product, go to www.altera.com/mysupport. For additional information about Altera products, consult the sources shown below.

Information Type	USA & Canada	All Other Locations
Technical support	www.altera.com/mysupport/	www.altera.com/mysupport/
	(800) 800-EPLD (3753) (7:00 a.m. to 5:00 p.m. Pacific Time)	+1 408-544-8767 7:00 a.m. to 5:00 p.m. (GMT -8:00) Pacific Time
Product literature	www.altera.com	www.altera.com
Altera literature services	literature@altera.com	literature@altera.com
Non-technical customer service	(800) 767-3753	+ 1 408-544-7000 7:00 a.m. to 5:00 p.m. (GMT -8:00) Pacific Time
FTP site	ftp.altera.com	ftp.altera.com

Typographic Conventions

This document uses the typographic conventions shown below.

Visual Cue	Meaning
Bold Type with Initial Capital Letters	Command names, dialog box titles, checkbox options, and dialog box options are shown in bold, initial capital letters. Example: **Save As** dialog box.
bold type	External timing parameters, directory names, project names, disk drive names, filenames, filename extensions, and software utility names are shown in bold type. Examples: $\mathbf{f_{MAX}}$, **\qdesigns** directory, **d:** drive, **chiptrip.gdf** file.
Italic Type with Initial Capital Letters	Document titles are shown in italic type with initial capital letters. Example: *AN 75: High-Speed Board Design.*
Italic type	Internal timing parameters and variables are shown in italic type. Examples: t_{PIA}, $n + 1$. Variable names are enclosed in angle brackets (< >) and shown in italic type. Example: *<file name>*, *<project name>***.pof** file.
Initial Capital Letters	Keyboard keys and menu names are shown with initial capital letters. Examples: Delete key, the Options menu.
"Subheading Title"	References to sections within a document and titles of on-line help topics are shown in quotation marks. Example: "Typographic Conventions."
`Courier type`	Signal and port names are shown in lowercase Courier type. Examples: `data1`, `tdi`, `input`. Active-low signals are denoted by suffix `n`, e.g., `resetn`. Anything that must be typed exactly as it appears is shown in Courier type. For example: `c:\qdesigns\tutorial\chiptrip.gdf`. Also, sections of an actual file, such as a Report File, references to parts of files (e.g., the AHDL keyword `SUBDESIGN`), as well as logic function names (e.g., `TRI`) are shown in Courier.
1., 2., 3., and a., b., c., etc.	Numbered steps are used in a list of items when the sequence of the items is important, such as the steps listed in a procedure.
■ ● •	Bullets are used in a list of items when the sequence of the items is not important.
✓	The checkmark indicates a procedure that consists of one step only.
	The hand points to information that requires special attention.
	The caution indicates required information that needs special consideration and understanding and should be read prior to starting or continuing with the procedure or process.
	The warning indicates information that should be read prior to starting or continuing the procedure or processes
↵	The angled arrow indicates you should press the Enter key.
	The feet direct you to more information on a particular topic.

1. About This Kit

Introduction

The Transceiver SI Development Kit, Stratix® II GX Edition provides everything you need to develop and test a complete signal integrity system based on the Stratix II GX EP2SGX90 device.

This chapter briefly describes the kit's features and documentation including:

- The Stratix II GX EP2SGX90 signal integrity development board
- Quartus® II Software, Development Kit Edition (DKE)
- Reference design
- MegaCore® IP Library CD-ROM

Kit Features

The Transceiver SI Development Kit, Stratix II GX Edition features:

- *The Stratix II GX EP2SGX90 Signal Integrity Development Board*—a prototyping platform that allows you to develop and prototype high-speed bus interfaces as well as evaluate Stratix II GX transceiver performance.

For specific information about board components and interfaces, refer to the *Stratix II GX Signal Integrity Development Board Reference Manual*.

- *Reference Design*—The reference design is useful for a variety of hardware applications and lets you quickly begin board prototyping and device verification.

- *Transceiver SI Development Kit Application & Drivers*—The kit's application and drivers allow you to customize board designs by choosing transceiver settings from a wide list of categories.

- *Quartus II Software, Development Kit Edition* (DKE)—The Quartus II software provides a comprehensive environment for system-on-a-programmable-chip (SOPC) design. The Quartus II software integrates into nearly any design environment, with interfaces to industry-standard EDA tools. The kit includes:
  - The SOPC Builder system development tool
  - A one-year Quartus II software license, Windows platform only

The Quartus II DKE software license allows you to use the product for 12 months. After 12 months, you must purchase a renewal subscription to continue using the software. For more information, refer to the Altera® website at **www.altera.com**.

- *MegaCore IP Library CD-ROM*, version 5.0—This CD-ROM contains Altera IP MegaCore functions. You can evaluate the MegaCore functions using the OpenCore® Plus feature, which allows you to do the following:
  - Simulate the behavior of a MegaCore function within your system
  - Verify the functionality of your design, as well as quickly and easily evaluate its size and speed
  - Generate time-limited device programming files for designs that include MegaCore functions
  - Program a device and verify your design in hardware

You only need to purchase a license for a MegaCore function when you are completely satisfied with its functionality and performance, and want to take your design to production.

The OpenCore Plus hardware evaluation feature is an evaluation tool for prototyping only. You must purchase a license to use an Altera IP function in production designs.

Documentation

The Transceiver SI Development Kit, Stratix II GX Edition contains the following documents:

- *Readme file*—Contains special instructions and points to the kit's documentation.
- *Transceiver SI Development Kit, Stratix II GX Edition Getting Started User Guide*—Describes how to start using the kit (this document).
- *Stratix II GX EP2SGX90 Signal Integrity Development Board Reference Manual*—Provides specific information about the board's components and interfaces, steps for using the board, and pin-outs and signal specifications.

2. Getting Started

Introduction

The Transceiver SI Development Kit, Stratix® II GX Edition is a complete signal integrity prototyping and testing kit based on the Stratix II GX device. With this kit, you can perform device qualification testing, transceiver performance testing at data rates ranging from 622 Mbps to 6.375 Gbps, and characterization testing of high-speed serial interfaces. You can also configure the FPGA with one of the kit's pre-defined designs.

In addition to providing a signal integrity development board, the kit also includes all of the hardware and software development tools, as well as the documentation and accessories you need to begin developing signal integrity systems using the Stratix II GX device.

This user guide will familiarize you with the contents of the kit and walk you through setting up a signal integrity development environment.

In this guide, you will do the following:

- Inspect the contents of the kit
- Install the development tools software
- Set up licensing
- Connect the cables to the board and your computer
- Setting the clock circuit switches
- Test transceiver performance using pre-defined designs
- Use the demo application to change transceiver parameters and observe performance
- Measure signal eye diagrams on differential data streams

Before You Begin

Before using the kit or installing the software, be sure to check the kit's contents and inspect the board to verify that you received all of the items listed in this section. If any of the items are missing, contact Altera® before you proceed. You should also verify that your computer's hardware and software meet the kit's system requirements.

Check the Kit's Contents

The Transceiver SI Development Kit, Stratix II GX Edition contains the following items:

- Stratix II GX transceiver signal integrity development board with an EP2SGX90EF1152C3NES Stratix II GX device (ordering code: DK-SI-2SGX90N)
- *Transceiver SI Development Kit, Stratix II GX Edition CD-ROM*, version 1.0.0, which includes:
  - Reference design
  - Stratix II GX signal integrity development kit application and device driver
- One-year license of Quartus® II Software Development Kit Edition (DKE), Windows only platform
- *MegaCore® IP Library CD-ROM*
- On-line training module, offering signal integrity and board layout guidelines
- USB-Blaster™ download cable
- Power supply and adapters for North America, Europe, the United Kingdom, and Japan
- Complete documentation
  - *Transceiver SI Development Kit, Stratix II GX Edition Getting Started User Guide* (this document)
  - *Stratix II GX EP2SGX90 Transceiver Signal Integrity Development Board Reference Manual*

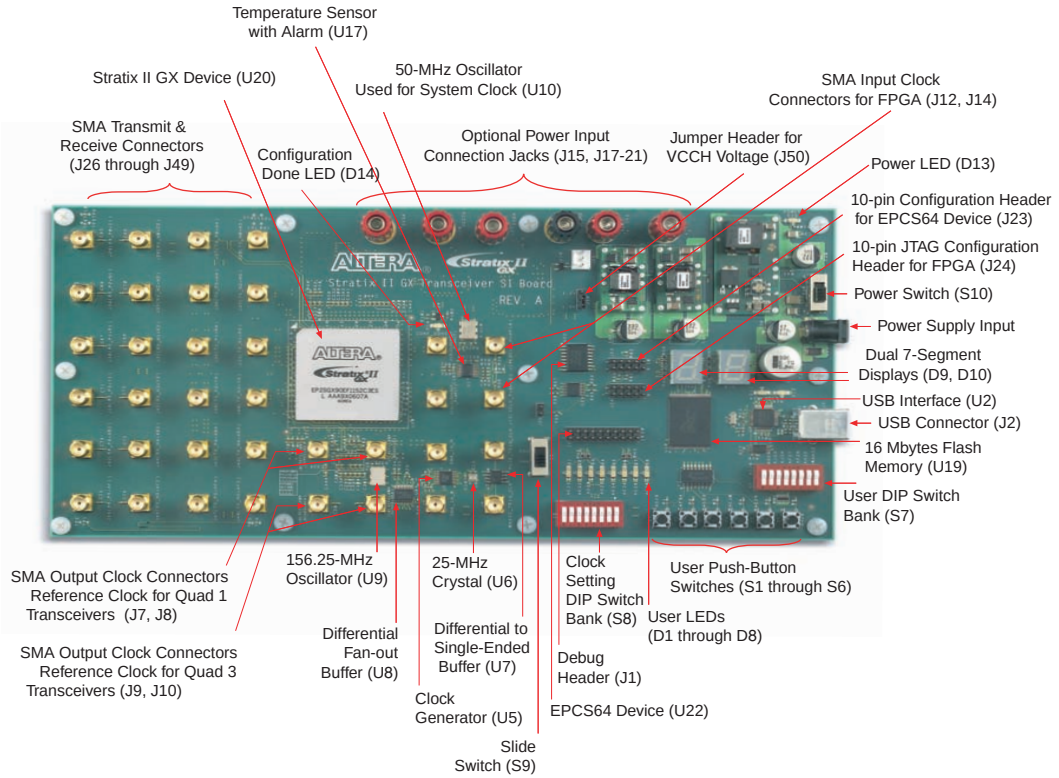
Inspect the Board

Place the board on an anti-static surface and inspect it to ensure that it has not been damaged during shipment. Verify that all components are on the board and appear intact.

Without proper anti-static handling, the Stratix II GX transceiver signal integrity development board can be damaged.

Figure 2–1 shows the Stratix II GX EP2SGX90 transceiver signal integrity development board.

Figure 2–1. Stratix II GX Transceiver Signal Integrity Development Board



Refer to the *Stratix II GX EP2SGX90 Transceiver Signal Integrity Development Board Reference Manual* (available on the *Transceiver SI Development Kit, Stratix II GX Edition CD-ROM*) for information on the board's components.

Hardware Requirements

All of the hardware that you need to use the board is provided with the Transceiver Signal Integrity Development Kit, Stratix II GX Edition.

Software Requirements

To use the kit's demo application, you must be running Windows XP.

Install the following software before you begin developing designs for the kit:

- The Quartus II software version 6.0. See "Installing the Quartus II Software and MegaCore Functions" on page 2–7.
- Internet Explorer 4.01 with Service Pack 2 or later to use Quartus II Help. You need a web browser to register the Quartus II software and request license files.

To license the Quartus II software, you will need:

- Your network identification card (NIC) ID.
- The kit's serial number, which is adhered to both the outside of the development kit's box and the CD-ROM.

Your NIC ID is a 12-digit hexadecimal number that identifies your computer. Networked (or floating-node) licensing requires a NIC ID or server host ID. When obtaining a license file for network licensing, you should use the NIC ID from the computer that will issue the Quartus II licenses to distributed users over a network. You can find the NIC ID for your card by typing `"ipconfig /all"` at a command prompt. Your NIC ID is the number on the physical address line, without the dashes.

Quartus II System Requirements

To use the *Transceiver SI Development Kit, Stratix II GX Edition CD-ROM* with the Quartus II software provided with the kit, your system must meet the Quartus II software minimum requirements.

For system requirements, refer to the *Quartus II Installation & Licensing for PCs* at **www.altera.com**.

Software Installation

The instructions in this section explain how to install the following:

- *Transceiver SI Development Kit, Stratix II GX Edition CD-ROM*
- Transceiver SI Development Kit, Stratix II GX Edition demo application and drivers
- The Quartus II Software, Development Kit Edition, including MegaCore functions from the MegaCore IP Library CD-ROM

Installing the Transceiver SI Development Kit, Stratix II GX Edition CD-ROM Contents

The *Transceiver SI Development Kit, Stratix II GX Edition CD-ROM* contains the following items:

- Transceiver SI Development Kit, Stratix II GX Edition GUI application and drivers
- Example design programming files
- *Transceiver SI Development Kit, Stratix II GX Edition Getting Started User Guide* (this document)
- *Stratix II GX EP2SGX90 Transceiver Signal Integrity Development Board Reference Manual*

Before you can compile the reference design, you must install the MegaCore IP Library CD-ROM.

To install the *Transceiver SI Development Kit, Stratix II GX Edition CD-ROM*, perform the following steps:

Insert the *Transceiver SI Development Kit, Stratix II GX Edition CD-ROM* into your CD-ROM drive and double click the **SIIGX_SI_Kit-v1.0.0** file. Follow the online instructions to complete the installation process.

The installation program copies the Transceiver SI Development Kit, Stratix II GX Edition files to your hard-disk, installs the software driver and application, and creates an icon in **Programs > Altera > Stratix II GX Signal Integrity Kit v1.0.0** (Windows Start menu), which you can use to launch the Windows development kit GUI.

When the installation is complete, the Transceiver SI Development Kit, Stratix II GX Edition installation program creates the directory structure shown in Figure 2–2, where <*path*> is the Transceiver SI Development Kit, Stratix II GX Edition installation directory.

Figure 2–2. Transceiver SI Development Kit Installed Directory Structure

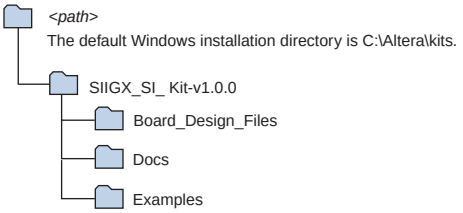


Table 2–1 lists the file directory names and a description of their contents.

Table 2–1. Installed File Directory Names and Description of Contents

Directory Name	Description of Contents
Board_Design_Files	Contains the board design and production test files. You can use the board design files as a starting point for creating your own prototype board.
Docs	Contains the documentation related to the development kit.
Examples	Contains the example design files including open-source HDL, Quartus II synthesis and simulation files for the Transceiver SI Development Kit, Stratix II GX Edition.

Installing the Transceiver SI Development Kit, Stratix II GX Edition Demo Application and Drivers

This section explains how to download and install the kit's demo application and drivers.

☞ If you receive an "`Application Error`" message when launching the demo application, please install **version 1.1 or later versions of the .NET** framework. Some Windows versions do not have runtime DLL for the .NET application. The .NET framework application can be downloaded from the following link:
http://www.microsoft.com/downloads/details.aspx?FamilyId=262D25E3-F589-4842-8157-034D1E7CF3A3&displaylang=en

- *Demo Application* — Download the demo application, **StratixIIGX_GUI.exe**, to a location on your hard drive.
- *Virtual COM Port (VCP) Driver* — For VCP driver installation instructions, go to the Future Technology Devices International (FTDI) web site (**www.ftdichip.com**) and search for the appropriate version of either the FT2232C or FT2232L device driver. The

appropriate version depends on the operating system that you are using. For example, Windows XP users need either the 1.0.2176 or the latest version.

- *Demo Driver* — For demo driver installation instructions, go to the FTDI web site (**www.ftdichip.com**) and search for the appropriate instructions based on the operating system that you are using.

Installing the Quartus II Software and MegaCore Functions

Refer to *Installing the Quartus II Software in the Quartus II Installation & Licensing Manual for PCs* for software installation instructions. After installing the software, request and install a license to enable it.

For information on obtaining a license file, refer to "Licensing Considerations".

To use the Quartus II software included with the kit, you must first obtain a license file. A one year Quartus II DKE software license is included with the kit.

During the installation of the Quartus II software, you are given the option to install the MegaCore IP Library. When prompted to do so, choose to install the MegaCore IP Library and follow the on-screen instructions.

Licensing Considerations

Before using the Quartus II software, you must request a license file from the Altera web site at **www.altera.com/licensing** and install it on your computer. When you request a license file, Altera emails you a **license.dat** file that enables the software.

To obtain a license, perform the following steps.

1. Point your web browser to the Altera web site at **www.altera.com/licensing**.
2. In the **Development Kit Licensing** list, select **Licensing for RoHS Compliant Development Kits**.
3. Follow the on-line instructions to request your license. A license file is emailed to you.

Before installing your license, close the following software if it is running on your computer:

- The Quartus II software
- The MAX+PLUS® II software

- The LeonardoSpectrum™ synthesis tool
- The Synplify software
- The ModelSim® simulator
- The Precision RTL Synthesis Software

4. To install your license, refer to *Specifying the License File* in the *Quartus II Installation & Licensing Manual for PCs*, which is included with the kit.

Connect the Cables to the Board and Computer

The instructions in this section explain how to set up the following hardware:

- USB-Blaster download cable
- SMA cable
- Power supply cable

USB-Blaster Cable

Connect the USB-Blaster cable's 10-pin female plug to the Stratix II GX device's JTAG header on the Stratix II GX EP2SGX90 transceiver signal integrity development board (J24), and connect the other end to the USB port on your computer. This approach allows you to directly configure the Stratix II GX device using an SRAM Object File (**.sof**). The kit's reference design includes a SOF for directly configuring the Stratix II GX device.

When connecting the JTAG side of the USB-Blaster cable, connect the marker line on the cable to pin 1 of the header (J24). Pin 1 of J24 is numbered on the board.

The USB-Blaster download cable driver must be installed before the USB-Blaster download cable can be used.

For information about installing the USB-Blaster download cable driver included with the Quartus II software, refer to the *USB-Blaster Download Cable User Guide*. The driver files are installed at <*quartus-install-dir*>**\drivers\usb-blaster**.

SMA Cable

The ends of the SMA cable can be connected to the SMA clock input connector.

Power Supply Cable

Connect the power cable to the board and plug the other end into a power outlet. To power up the board, place the power switch (S10) in the *ON* position. When power is supplied to the board, the LED (D13) illuminates.

After the board powers up, the on-board flash memory, which ships pre-programmed with the factory design, automatically configures the Stratix II GX device. The CONF DONE LED (D14) illuminates, signaling that the Stratix II GX device is configured.

☞ If the board does not power up after the power cable is connected, make sure that the power switch (S10) is in the *ON* position.

Setting the Clock Circuit Switches

Set the DIP switch S8 and slide switch S9 per the instructions listed in Table 2–2.

Table 2–2. Setting the Clock Circuit Switches, Note (1)

S8-1, S8-2, and PCIe Clk			S8-3, S8-4 and PCIe Clk			S8-5 and PCIe Clk		S8-6 and Basic Clk	
S8-1	S8-2	PCIe Clk (U5)	S8-3	S8-4	PCIe Clk (U5)	S8-5	PCIe Clk (U5)	S8-6	Basic Clk (U8)
Low	Low	25 MHz	Low	Low	±25%	High	Enable	High	Enable
High	Low	100 MHz	High	Low	-0.5%	Low	Disable	Low	Disable
Low	High	125 MHz	Low	High	-0.75%	—	—	—	—
High	Low	200 MHz	High	High	No spread	—	—	—	—

Note to Table 2–2:
(1) When using the clock speed DIP switch bank (S8), set switches 1-5, 7, and 8 in the closed position, and switch 6 in the open position.

☞ To use the on board oscillator, the slide switch (S9) needs to be in the OSC position. However, to use the SMA connectors J5 and J6, the slide switch needs to be in the SMA position. The I/O standard of the pattern generator should be set to LVPECL, LVDS, LVHSTL, SSTL, or the HCSL level.

Test the Transceiver Performance Using Pre-Defined Designs

The kit provides pre-defined test designs and an easy-to-use demo application with a custom graphical user interface (GUI). The demo application's GUI allows extensive transceiver channel testing at various data rates and clocking schemes.

This section provides:

- Pre-defined test design results
- Demo application GUI tutorial

Pre-Defined Test Designs

Altera engineers created a set of pre-defined test designs for you to evaluate Stratix II GX device transceiver performance and board features. As you can tell from the data listed in Table 2–3, the results can vary dramatically when choosing from various clocking schemes and data rates.

Table 2–3 lists the default transceiver settings.

Table 2–3. Transceiver Test Design Results

File Name	Quad 1 Channel 1 Data Rate (Gbps)	Quad 2 Channel 1 Data Rate (Gbps)	Quad 3 Channel 1 Data Rate (Gbps)	Clocking Scheme *Note (1)*
gxbguictrl_top1.sof	6.25	3.125	6.25	Clock from 156.25-MHz oscillator
gxbguictrl_top2.sof	5	2.5	5	Clock from 156.25-MHz oscillator

Note to Table 2–3:

(1) The clock input can also be given from an external source. The frequency of the clock should be selected such that the data rate in Quads 1 and 3 should be within the 6.375 Gbps - 3.126 Gbps range. For Quad2 the data rate should be within the 3.125 Gbps-622 Mbps range. See Table 2–4.

Refer to the section "Connect the Cables to the Board and Computer" on page 2–8 for information on using the JTAG interface when configuring the Stratix II GX device with one of the pre-defined designs. The CONF DONE LED (D14) illuminates upon successful device configuration. Also, the 7-segment display shows the programmed SOF/POF number. For example, for the **gxbguictrl_top1.sof** the 7-segment display indicates the SOF with `01`, and with the **gxbguictrl_top2.sof** the 7-segment display indicates the SOF with `02`.

Table 2–4 lists the allowed input clock frequency range for the various GUI channels.

Table 2–4. Input Clock Frequency Range for GUI Channels

GUI Channel Number	Data Rate Range	Clock Frequency Range
Ch0, Ch5	6.375 Gbps – 3.126 Gbps	159.375 MHz – 78.15 MHz
Ch1..Ch4	3.125 Gbps – 622 Mbps	156.25 MHz – 62 MHz

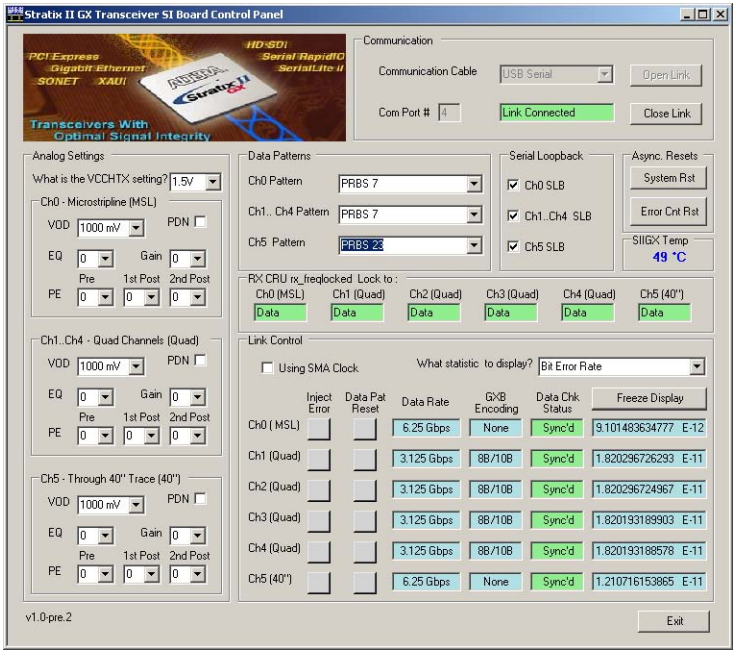
Demo Application GUI Tutorial

The demo application's GUI provides an easy-to-use control panel where you can select various transceiver settings and observe the results. This feature allows you to customize your board design by choosing transceiver settings from the following categories (see Figure 2–3):

- Analog
- Communication cable
- Data patterns
- Serial loopback
- Resets
- Clock recovery unit (CRU)
- Link control

To execute the demo application's GUI, double-click the **StratixIIGX_GUI.exe** file, which is available on the *Transceiver SI Development Kit, Stratix II GX Edition CD-ROM*.

Figure 2–3. Demo Application Control Panel WIndow



Before walking through the GUI tutorial, you should configure the Stratix II GX device with one of the pre-defined SOFs listed in Table 2–3.

Analog Settings

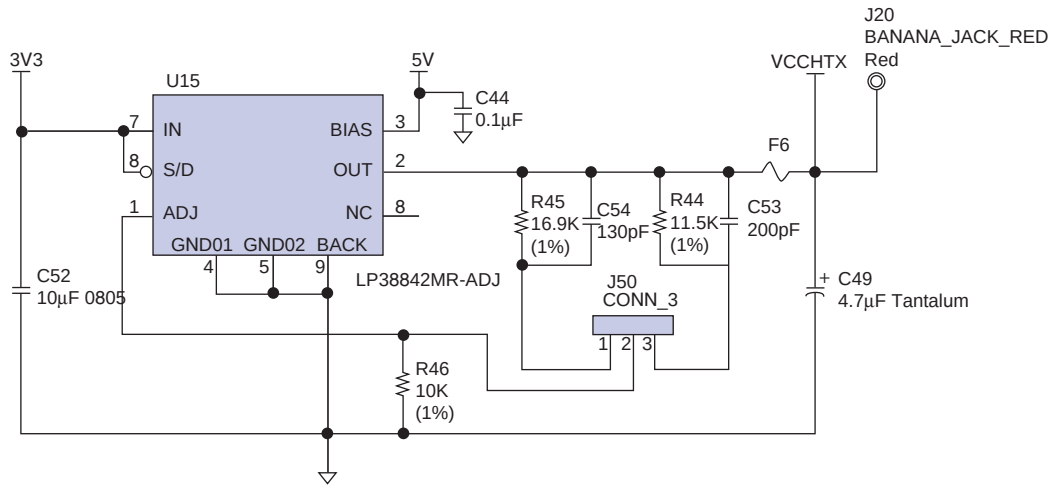
The left side of the control panel window provides the physical media attachment sublayer (PMA) setting values that represent the different transceiver Quads and are based on the VCCHTX setting. The VCCHTX setting should correspond with jumper header (J50) settings. See Table 2–5.

Table 2–5. Jumper Header (J50) Connections and VCCHTX Values

Jumper Header (J50) Connection	VCCHTX
Pins 1 and 2	1.5 V
Pins 2 and 3	1.2 V

Figure 2–4 shows the jumper header connections and corresponding VCCHTX values.

Figure 2–4. Jumper Header Connections and Corresponding VCCHTX Values



Before powering up the board, the VCCHTX jumper settings should be specified.

The following list defines the analog setting parameters in the control panel window:

- VOD = output driver voltage
- EQ = equalization
- Gain = DC gain
- PE = pre-emphasis
  - In the PE setting list, **Pre**, **1st Post**, and **2nd Post** settings represent different taps.
- PDN = Setting the PDN performs a power down on the Quad.

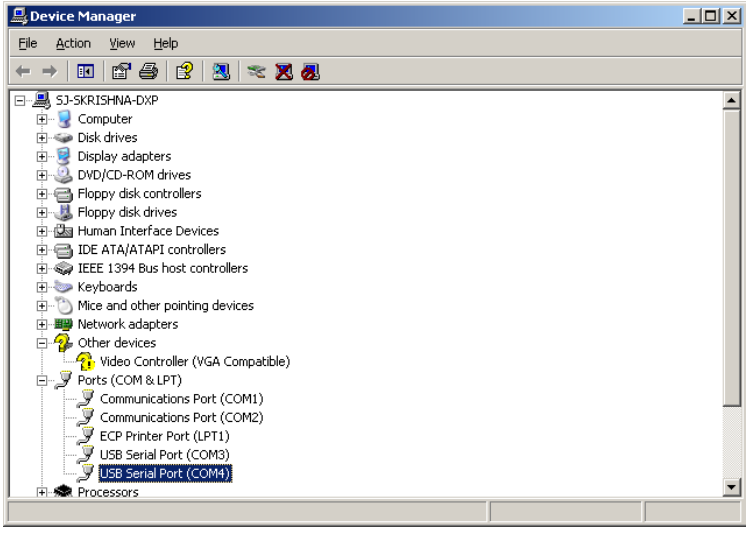
Communication Settings

The top right-hand side of the control panel window provides the following **Communication** settings:

- **Communication Cable**—This list displays the different physical interconnect options to communicate with the board. Currently, **USB Serial** is supported.

- **COM Port #**—When the driver is installed, the COM Port values are listed under **Ports (COM and LPT)** in the Windows **Device Manager** window (go to **Start** > **Control Panel** > **Administrative Tools** > **Computer Management** > **Device Manager**). See Figure 2–5. The highest COM port number listed under **Ports (COM and LPT)** is required to be used in the **COM Port #** box.
- **Open Link** and **Close Link**—When you click **Open Link** or **Close Link,** the link with the board and the status of the connection is shown under **Display Adapters** in the **Device Manager** window (see Figure 2–5).

Figure 2–5. Device Manager Window



When the SOF is downloaded to the hardware, the link from the GUI to the board should be closed.

Data Pattern Settings

The top center of the control panel window provides the following **Data Pattern** settings:

- **Ch0 Pattern**
- **Ch1., Ch4 Pattern**
- **Ch5 Pattern**

Three different data pattern generators—PRBS7, PRBS23, and high frequency alternate `1`s and `0`s—are available for all channels. Data checking is only available for the PRBS7 and PRBS23 pattern generators. Error statistics are reported to the demo application by the checkers.

Serial Loopback Settings

Immediately to the right of the **Data Pattern** settings are the **Serial Loopback** settings. Serial loopback is available for all the channels and can be controlled during run time.

After the serial loopback status in the GUI is changed, the **Data Chk Status** box may indicate **Unsync'd** for some channels due to the asynchronous nature of the serial loopback signal. In this scenario, the **Data Pat Rst** should be asserted to synchronize the error checker with the transmitted data.

Reset Settings

Immediately to the right of the **Serial Loopback** settings are the **Reset** settings, which are defined below:

- **System Rst**—Reset for the transceiver

After **System Rst** is asserted, the **Data Chk Status** box may show **Unsync'd** for some channels due to the asynchronous nature of the reset. In this scenario, the **Data Pat Rst** should be asserted to synchronize the error checker with the transmitted data.

- **Error Cnt Rst**—Reset for all the error counters to zero
- **SIIGX Temp**—This field shows the Stratix II GX device's junction temperature.

Also, when the you change the data patterns in the **Data Patterns** field (depending on the specified channel), the error counters will be reset. For example, in the **Ch1.,Ch4 Pattern** field, if you change **PRBS7** to **PRBS23**, the error counters are reset for all four channels.

RX CRU Rx_Freqlocked Lock to Settings

The middle center of the control panel window is the **RX CRU rx_freqlocked Lock to**: settings. This field shows whether the transceiver's CRU is locked to the reference clock or to the data. When the

transceiver locks to the incoming data, the **RX CRU rx_freqlocked Lock to**: field displays **Data** indicating that the receiving PLL has recovered the clock from the incoming data.

Link Control Settings

The bottom center of the control panel window provides the **Link Control** settings. The Link Control settings include the following options:

- **Using SMA Clock**—When the **Using SMA Clock** field is selected, the serial data rate is shown as a multiplication factor of the clock frequency for all channels. The multiplication factor is based on the channel width used in the test design. When the external clock is used to run the transceiver, the *P* and *N* differential outputs of the clock source should be connected to SMA connectors J5 and J6 respectively and switch S9 should be set to the SMA position.
- **What statistic to display?**—This list displays the bit error rate, number of bits received, number of errors received, and error rate slope. The error rate slope provides an approximate indication of the increasing and decreasing trend of the number of errors received.
- **Inject Error**—This button injects errors in the channels. Every time this button is asserted, a one bit error is introduced.
- **Data Pat Rst**—Reset for the data pattern generators and checkers.
- **Data Rate**—Based on the selected test design, the **Data Rate** box displays the serial data rate of the transceiver channels.
- **GXB Encoding**—The GXB Encoding box displays whether the data sent by the test design is 8B/10B encoded.

Data Chk Status—Before transmitting the data patterns, the pattern generators transmit a pre-defined header byte to enable the error checkers. Upon receiving the pre-defined header byte, the error checker monitors for errors in the received pattern. The **Data Chk Status** box displays the following:

- **Sync'd** status displayed in green indicates that the error checker has received the pre-defined header byte and no errors are detected.
- **Unsync'd** status displayed in gray indicates that the error checker has not received the pre-defined header byte. When this situation occurs, you should ensure that the transmitter of the channel showing **Unsync'd** is connected to the receiver channel by external cable or by internal serial loopback. Still, when

sending a high frequency data pattern, the **Data Chk Status** box will also show **Unsync'd**. This is because the error checker does not monitor for high frequency error data patterns.
- **Error** status indicates that the error checker is detecting errors in the received pattern.

- **Freeze Display**—When the **Freeze Display** button is pressed, the display field is not changed. However the counting is not stopped. When the **Unfreeze Display** is pressed, the current running values are shown.

Measuring Signal Eye Diagrams of Transmitted Data

The on-board EP2SGX90E device's embedded transceivers support up to 12 transceiver channels. Each transceiver channel has a transmitter and a receiver. Designers can preset Stratix II GX transceiver functions using the Quartus II software.

Stratix II GX devices are designed with superior pre-emphasis and equalization. Pre-emphasis conditions the signal prior to transmission resulting in an open eye at the far end, while equalization opens the eye in the receiver. Pre-emphasis and equalization ensure optimal signal integrity.

In this section, you will walk through the process of measuring signal eye diagrams of transmitted data.

The following lists the required test equipment:

- Sampling oscilloscope with Infinite Persistence display capability, such as Tektronix TDS8000
- Two length matched 50-Ω SMA cables for transmission data out (TX_Px and TX_Nx) with at least 18GHZ bandwidth.
- One 50-ohm SMA cable for the Trigger input to the oscilloscope.

For information on using Altera megafunctions to customize transceiver channels, refer to the *Stratix II GX alt2gxb Megafunction User Guide* chapter of the *Stratix II GX Device Handbook, Volume 2*.

Set Up The Testing Environment

This section provides the steps in setting up a testing environment. Depending on the design running on the development board, one or more of the six transmitter channels will transmit serial data.

Assuming the design is successfully running on the Stratix II GX transceiver signal integrity board, the following steps walk you through the process of measuring eye-diagrams of transmitted data.

1. Connect a 50-Ω SMA cable between the TX_P0 through TX_P5 connectors on the board (depending on the channel for which the eye-diagram needs to be measured) and Ch1 on the TDS8000 sampling module.

   The TX_P5 channel has a 40 inch trace between the FPGA serial data output pin and the SMA connector.

2. Connect an equal length 50-Ω SMA cable between the TX_N0 and TX_N5 connectors on the board and Ch2 on the TDS8000 sampling module.

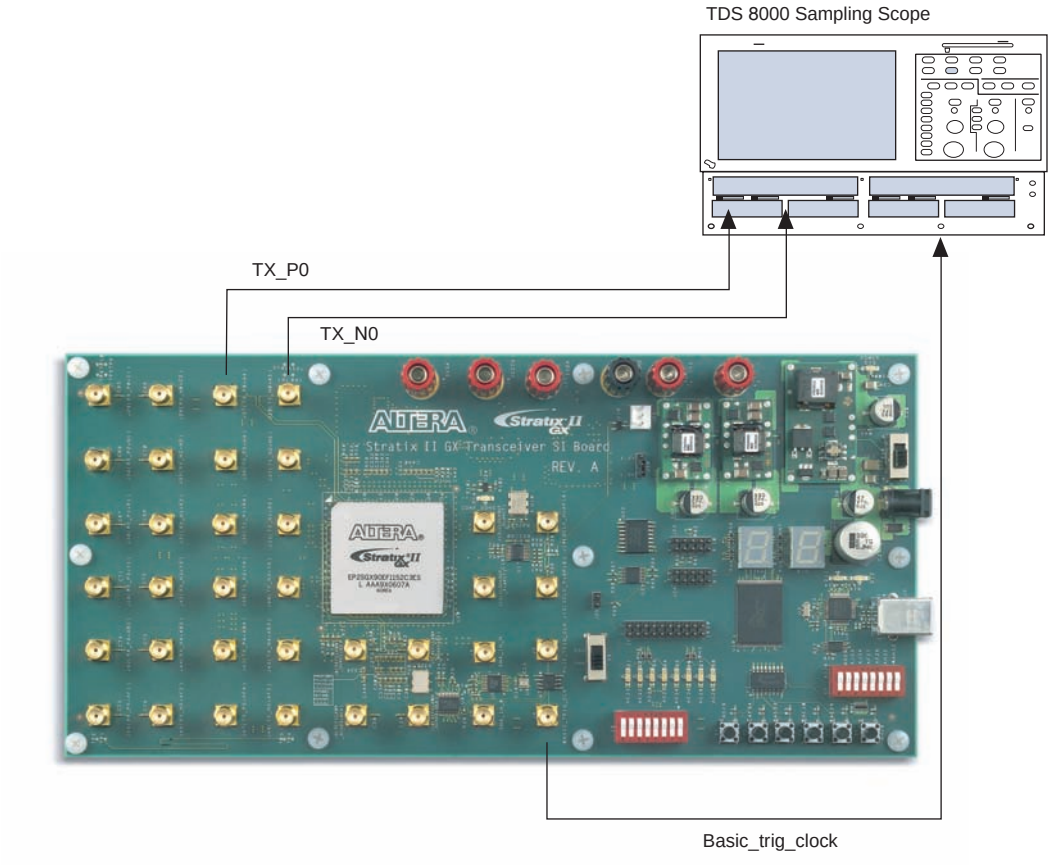
   The TX_N5 channel has a 40 inch trace between the FPGA serial data output pin and the SMA connector.

3. Connect a 50-Ω SMA cable between the clock trigger output (J3 or J4 depending on which clock is specified as the design's refclk) and the direct trigger input on the TDS8000 front panel.

4. Customize the TDS8000 to measure the eye diagram on differential data streams. You can do this by using the math utility provided on the sampling oscilloscope. Setting up the math utility to measure eye diagrams on Ch1-Ch2 effectively gives a differential eye measurement (See Figure 2–6).

Use the DC block for high-speed signals going into the oscilloscope, e.g., TX_P0, and TX_N0. For the trigger clock output from the Stratix II GX transceiver signal integrity board, use the DC block. Also use the attenuator depending on the allowable input voltage range of the oscilloscope.

Figure 2–6. Connecting the TDS8000 Sampling Oscilloscope



For more information, please refer to the *Tektronix TDS8000 User Guide* or reference manual of the sampling oscilloscope used.

Appendix A. Non-GUI Based Example Design

Design Features

This manually-controlled (non-GUI based) example is a one channel design using the microstrip transceiver quad at 6.25 Gbps. The input clock frequency is 156.25 MHz and the interface is 40 bits wide. The `TX_P0` is connected to `A4` and `RX_P0` to `C1`. The other transceiver quads that are not used are powered off. Data patterns supported are PRBS23, PRBS7, and the high frequency pattern (`1010`).

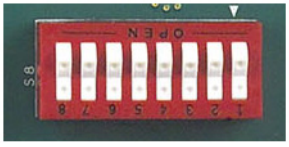
The checkers are only available for the PRBS23 and PRBS7 data patterns.

The following parameters can be controlled during run-time:

- Preemphasis—Main tap (The other tap controls are not available.)
- Equalization
- DC gain
- VOD
- Data pattern select
- Serial loopback

The parameters are controlled using a combination of DIP switches and push-button switches. See Table A–1. The on-board frequency rate used for the design is 156.25 MHz. Please set switch 6 in the clock setting DIP switch bank (S8) to OPEN. Figure A–1 shows all the switches in the closed position.

Figure A–1. Clock Setting DIP Switch Bank (All Switches In Closed Position)



General User Interfaces

This section describes the following general user interfaces, which provide direct feedback regarding board, clocking, and signal activity:

- LED display
- 7-segment display
- DIP switches
- Push buttons

LED Display

Signals propagating to LEDs indicate board status. Table A–1 lists the signal name, description, width, board reference number, and the FPGA pin in which the signal is connected.

Table A–1. LED Display (Part 1 of 2)

Number	Signal Name	Description	Width	Board Reference Number	Connected to FPGA Pin Number
1	Tx_pll_locked	Shows whether the TX phase-locked loop (PLL) is locked to the input clock	1	D1	AE33
2	Rx_syncstatus	When ON, indicates that the receiver has acquired synchronization with the input data.	1	D2	AE32
3	Checker_synced	Indicates that the checker is checking for errors on the received data.	1	D3	AD26
4	Error_flag	The LED is ON for one second when an error is detected by the pattern checker. Shows the running error status.	1	D4	AD25
5	Error status_first_digit *(1)*	The LED is ON if the LSB[7:0] of the error counter reaches 0xFF. The LED is reset when clear_error_counter_switch is asserted.	1	D5	AD34
6	Error status_second_digit *(1)*	The LED is ON if the LSB[15:8] of the error counter reaches 0xFF. The LED is reset when clear_error_counter_switch is asserted.	1	D6	AE34
7	Error status_third_digit *(1)*	The LED is on if the LSB[23:16] of the error counter reaches 0xFF. The LED is reset when clear_error_counter_switch is asserted.	1	D7	AC29

Table A–1. LED Display (Part 2 of 2)

Number	Signal Name	Description	Width	Board Reference Number	Connected to FPGA Pin Number
8	`Serial_loopback`	The LED is ON when serial loopback is enabled	1	D8	AC28

Note to Table A–1:
(1) The first, second, and third digits display the approximate error count range.

7-Segment Display

The 7-segment displays are used to:

- Display the VOD, pre-emphasis, DC gain, and equalization values when reading or writing the PMA settings.

Refer to the "Write and Read PMA values" on page A–6 for more information.

- Display the design file name when the `system_reset` push button switch is asserted.
- Display the error count when `show_error_count` push button switch is asserted.

The VOD values shown by the 7-segment display indicates the value in mV when multiplied by 100. For example, to show a VOD of 200mV the 7-segment display shows 02. The display setting is for a VCCHTX of 1.5 V.

DIP Switches

The DIP switch S7 is used for controlling the different transceiver parameters. Table A–2 lists the DIP switch names and describes the individual switch functions. The DIP switch numbers are shown on the board's silkscreen.

To set a DIP switch in the open position, press the switch towards the OPEN side of the user DIP switch bank. To set a DIP switch in the closed position, press the switch towards the number side of the DIP switch bank.

Table A–2. DIP Switch Signal Names and Descriptions *Note (1)*

DIP Switch Name	Description	Width	Board Reference Number	Connected to FPGA Pin Number
Read and write PMA control	The switch is used to display or set the controllable parameters. The values are displayed in the 7-segment display, i.e., O = read VOD, preemphasis from the transceiver C = write VOD, preemphasis into the transceiver	1	1	AH33
PMA controls	Silkscreen number: 4 3 2 O O O – preemphasis (only main tap) O O C – VOD O C C – DC gain C C C – equalization The other silkscreen numbers are reserved. After this combination is set, push_button_PMA_control has to be pressed to set the values.	3	2, 3, 4	AH32, AF28, AF27
Data pattern select	The switch selects the data patterns. Switch position-silkscreen number: 6 5 C O – PRBS23 O C – PRBS7 O O – high frequency C C – reserved	2	5, 6	AJ34, AJ33
Serial loopback	The switch dynamically controls serial loopback. O = serial loopback ON C = serial loopback OFF	1	7	AG29
Reserved	—	1	8	AG28

Note to Table A-2:
(1) The C refers to the DIP switch in the closed position, and the O refers to the DIP switch in the open position.

Push Button Switches

Table A–3 lists the push button switch signal names, describes the functionality, lists the board reference numbers, and FPGA pin connection.

Table A–3. Push Button Switches

Push Button Switch Name	Description	Board Reference Number	Connected to FPGA Pin Number
resetn (system reset)	Performs a reset on the transceiver and also the entire design.	S1	AD28
generator_checker_reset_switch	Performs a reset on the data generators and error checkers. The push button will also reset the error counters.	S2	AF34
change_PMA_switch	Based on the selection of the PMA Controls DIP switch, the push button sets the value for either VOD, preemphasis, DC gain or equalization. Every time the push button is pressed, the value is incremented. When the maximum value is reached, the value starts from zero.	S3	AF33
insert_error_switch	Inserts one bit error in the transmit data.	S4	AE30
clear_error_counter_switch	The push button resets the error counters.	S5	AE29
show error count	Displays the most significant byte of the error. For example if the error count is 02FF, when the push button is asserted 02 is displayed *until* the button is de-asserted. Refer to Table A–1 on page A–2 for additional information.	S6	AH20

Write and Read PMA Values

This section walks you through setting up the example design's write and read PMA values.

Write PMA Values

Use the following steps to set up the example design:

1. Set `read_write_PMA_control` (DIP_sw[0]) to the closed position.
2. Set `PMA_controls` (DIP_sw[3,2,1]) DIP switch to preemphasis, VOD, equalization, or DC gain settings.

Refer to "DIP Switches" on page A–3 for the values.

3. Assert `Change_PMA_switch` push button switch (S3) to change the value of selected `PMA_control`.

Refer to the "Push Button Switches" on page A–5 for more information.

4. Observe the values in the 7-segment display. The value written in the transceiver is displayed.

The VOD values shown by the 7-segment display indicates the value in mV when multiplied by 100. For example to show a VOD of 200mV, the 7-segment display shows `02`. This display setting is for a VCCHTX of 1.5 V.

Read PMA Values

Use the following steps to set up the example design:

1. Set `read_write_PMA_control` (DIP_sw[0]) to the open position.
2. Set `PMA_controls` (DIP_sw[3,2,1]) DIP switch to preemphasis, VOD, equalization, or DC gain settings.

Refer to "DIP Switches" on page A–3 for the values.

3. Observe the values in the 7-segment display. The value read from the transceiver is displayed.

Design Walkthrough With Troubleshooting and Debugging Solutions

This section walks you through a design example and also provides troubleshooting and debugging solutions.

Design Walkthrough

The following steps walk you through an example sequence to run a PRBS23 with the values of VOD = 2, preemphasis = 1, DC gain = 1, and equalization = 3.

Please refer to "Stratix II GX Transceiver Signal Integrity Development Board" on page 2–3 for all component number references.

1. Power up the board.
2. If the on-board clock is used, ensure that the slide switch (S9) is in the oscillator position (OSC).
3. Set switch 6 of the clock setting DIP switch bank (S8) to OPEN.
4. Set switch 7 of the user DIP switch bank (S7) to OPEN for serial loopback.
5. To set the pattern generator to PRBS23, set switch 6 of the user DIP switch bank (S7) to closed and switch 5 to OPEN.
6. Set the VOD, preemphasis, DC gain, and equalization values.

Refer to "Write PMA Values" on page A–6.

7. This is an optional step. Refer to "Read PMA Values" on page A–6 to confirm whether the intended settings are written.
8. Assert the push button switch S2 to reset the data generators and checkers.
9. Check the status of LED's D1, D2, and D3. When all three LEDs are illuminated, the transaction is successful.

Troubleshooting Solutions

This section provides troubleshooting solutions. If your transaction is not successful, review the following troubleshooting suggestions:

- If the LED D1 is not illuminated, the system may not be receiving the clock cycles. Ensure that the slide switch (S9) is in the oscillator position (OSC). Also, ensure that switch 6 of the clock setting DIP switch bank (S8) is set to OPEN.

- If the LED D2 is not illuminated, the receiver cannot sync to the transmitted data. To remedy this problem:
  - Ensure that serial loopback is ON if external loopback is not completed.
  - If external loopback is completed, check the quality of the cables used.
  - Assert the `system_reset` push button switch.

- If the LED D3 is not ON, the data checker did not receive the expected data. To remedy this problem:
  - Ensure that the data pattern of the DIP switch is set to PRBS7 or PRBS23.

High frequency data patterns do not have a data checker. Therefore, the LED D3 will be off when high frequency patterns are used.

- If the display shows `EE`, the DIP switch selection for PMA_controls is not correct.

Debugging Using the SignalTap® II Embedded Logic Analyzer

In the kit's **Examples\SII_GX_SI_NonGUI_Design** directory there is a Quartus® II archive (**.qar**) file containing the example design project. The **design1.stp** file is part of the **.qar** file and contains a variety of debugging signals. The available signals are:

- All resets going into the transceivers
- Status signals from transceivers: `rx_freqlocked`, `rx_syncstatus`
- Input push button and DIP switch values
- Reconfiguration block signals
  - Inputs and outputs of VOD, preemphasis, equalization and DC gain values
  - Read, write, busy, and data valid signals
- Data generator and checker signals
  - Parallel data output to the transceiver

- Data pattern selected by the DIP switch, which have the following values:
  - `01`: PRBS23
  - `10`: PRBS7
  - High frequency pattern (`1010`)
- Receive side data to PRBS23 and PRBS7 checkers.
- Error count values for PRBS23 and PRBS7 checkers
- Lock signals for PRBS23 and PRBS7 checkers. This indicates that the checker matched the receive pattern with the expected data pattern.

Creating Your Custom Data Generators and Checkers

The **data_gen_checker_top_40bits.v** is the top level for the data generators and checkers. If you would like to create your own data generators and checkers, replace this module with your own module. The data output of this module should be connected to the `tx_datain` port of the transceiver instantiation (**alt2gxb_6G_6250.v**) in the top-level **design_s2gx_top_level.v**.